a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

2.(Amended) An [electro-optical] active matrix type display device comprising:

at least two transistors provided on an insulating surface in a decoder circuit of a driver circuit of said [electro-optical] active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

3.(Amended) An [electro-optical] active matrix type display device comprising:

at least two transistors provided on an insulating surface in a buffer circuit of a driver circuit of said [electro-optical] active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

6.(Amended) An [electro-optical] active matrix type display device comprising:

at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common

drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

8.(Amended) An [electro-optical] active matrix type display device comprising:

at least two transistors provided on an insulating surface in a driver circuit of said [electro-optical] active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

11.(Amended) The device of claim 1 wherein said [electro-optical] active matrix type display device [has] comprises a memory.

12.(Amended) The device of claim 1 wherein said [electro-optical] active matrix type display device [has] comprises a decoder.

13.(Amended) The device of claim 1 wherein said [electro-optical] active matrix type display device [is] comprises a display system.

D2

14.(Amended) The device of claim 2, wherein said [electro-optical] active matrix type display device [has] comprises a memory.

16.(Amended) The device of claim 2 wherein said [electro-optical] active matrix type display device [is] comprises a display system.

17.(Amended) The device of claim 3 wherein said [electro-optical] active matrix type display device [has] comprises a memory.

D3

18.(Amended) The device of claim 3 wherein said [electro-optical] active matrix type display device [has] comprises a decoder.

19.(Amended) The device of claim 3 wherein said [electro-optical] active matrix type display device [is] comprises a display system.

D4

26.(Amended) The device of claim 6 wherein said [electro-optical] active matrix type display device [has] comprises a memory.

27.(Amended) The device of claim 6 wherein said [electro-optical] active matrix type display device [has] comprises a decoder.

28.(Amended) The device of claim 6 wherein said [electro-optical] active matrix type display device [is] comprises a display system.

32.(Amended) The device of claim 8 wherein said [electro-optical] active matrix type display device [has] comprises a memory.

D5

33.(Amended) The device of claim 8 wherein said [electro-optical] active matrix type display device [has] comprises a decoder.

34.(Amended) The device of claim 8 wherein said [electro-optical] active matrix type display device [is] comprises a display system.

Please add new claims 71-75 as follows.

--71. The device of claim 1 wherein said active matrix type display device is a liquid crystal display device.

72. The device of claim 2 wherein said active matrix type display device is a liquid crystal display device.

D6

73. The device of claim 3 wherein said active matrix type display device is a liquid crystal display device.

74. The device of claim 6 wherein said active matrix type display device is a liquid crystal display device.

75. The device of claim 8 wherein said active matrix type display device is a liquid crystal display device.--